OBJECTIVES:

1- To fabricate Bipolar Junction Transistors.
2- To test the fabricated Bipolar Junction Transistors performance.

THE THEORY:

The diffused planar process remains one of the most important processes available for Large-Scale IC (LSI) fabrication. The aim of this experiment is the fabrication of Bipolar Junction Transistors (B.J.T.) using this process.

IC's fabricated using the planar processes have available on their top surfaces, the regions on which contacts are to be made. For instance, in our particular case we will be fabricating bipolar junction transistors on (N or P-type) silicon wafers. As can be seen in figure 1, the cross section of the transistors we will be fabricating, the base, emitter and collector regions will all be "accessible" at the top surface of the silicon substrate. Thus, once these regions have been formed in the substrate through the diffusion of appropriate impurities, aluminum contacts can be conveniently made to each of these areas on the wafer's top surface.

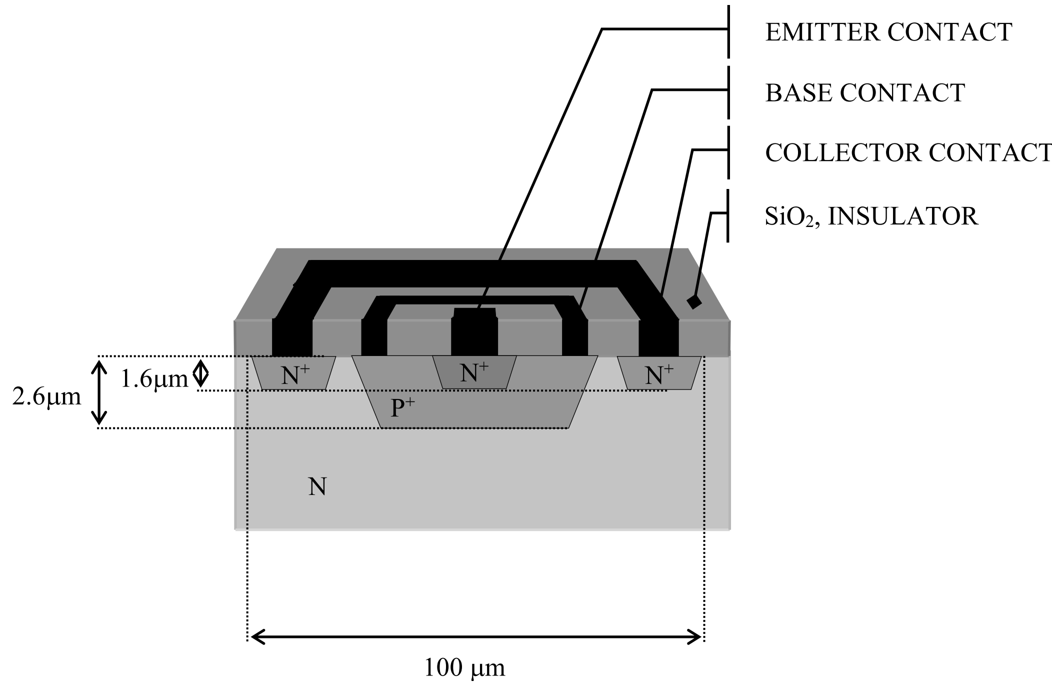
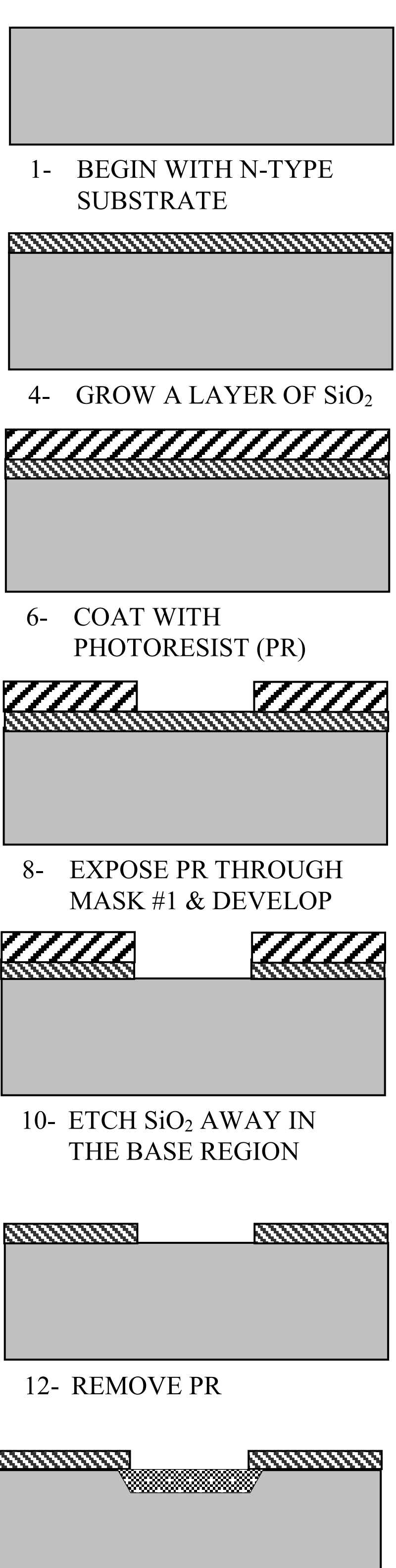


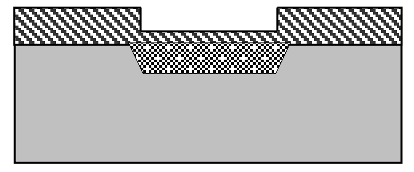
Figure 1- Cross-section of a diffused planar NPN transistor

The planar process is made possible due to the fact that silicon dioxide (SiO_2) may be grown on the silicon substrate and then selectively removed from designated areas through photolithographic and etching techniques. The oxide effectively keeps any

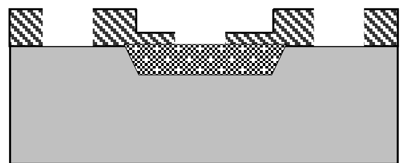
doping impurities from diffusing into the areas it covers and thus permits the formation of P or N regions over well defined areas on the substrate's surface. The oxide also serves to protect the junctions where they reach the surface of the sample from surface contamination and it also isolates the three contacts from each other. (SiO_2) is an excellent insulator.
Figure 2 shows the process steps required for the formation of a diffused planar NPN bipolar junction transistor. These are the steps that will be followed during the course of this experiment. Keep in mind that the figure 2 shows the formation of simply one transistor. But in fact, several such structures will be created over the surface of the substrate. We begin with an N-type substrate on which a layer of silicon dioxide is grown. The sample is then coated with photoresist, which is subsequently exposed through the "base mask" (mask #1) and developed. The SiO_2 is then etched away from the base-diffusion region and the remaining photoresist is stripped from the surface. Boron is diffused into the open "window" to form the P-type base and the surface is then re-oxidized. Using photolithography once again, the oxide is removed from those regions in which phosphorus is to be diffused using mask #2 to form the N-type emitter and collector regions. Once the phosphorus has been diffused to the appropriate depth, the entire surface of the "transistor" is re-oxidized in preparation for the metallization step. The sample is coated with photoresist once more, which is as before exposed through the metallization mask (mask #3) and developed. This time, after the oxide has been etched away from the designated areas, the photoresist is NOT removed from the sample's top surface. Aluminum is evaporated onto the entire surface with the resin still on it and the excess Al, which does not cover any contact area, is "floated off". This is done chemically with a solution that "swells up" the resin and dislodges the aluminum from the non-contact areas. This process is known as lift-off. After this process, aluminum is left only in the base, emitter and collector contact regions. The contacts are then alloyed to the Si substrate and device performance is finally tested.

Now we will describe all of the devices and the sub fabrication processes that we are going to encounter in this fabrication lab.

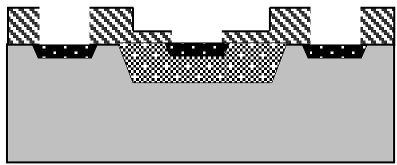




2- RE-OXIDATION OF SURFACE

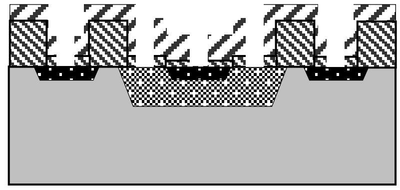


3- REMOVE SiO_2 USING MASK #2

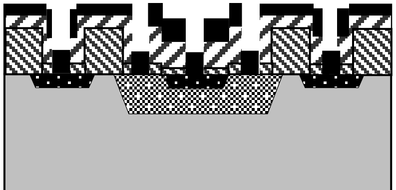


5- DIFFUSION (P) N-TYPE FOR EMITTER & COLLECTOR

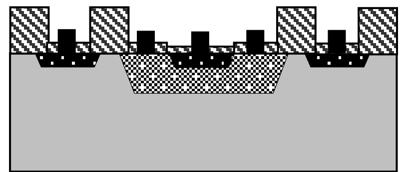
7- RE-OXIDATION OF SURFACE



9- REMOVE SiO_2 FROM E-B-C CONTACT AREAS (KEEP PR ON)



11- EVAPORATE Al ONTO THE SAMPLE



13- FLOAT OFF EXCESS Al & ALLOY CONTACTS

Figure 2- Process Steps: NPN planar transistor fabrication

THE CLEANING PROCESS:

Dust, sodium (Na), aluminum (Al), and native oxide, are the most known types of unwanted impurities that a sample may be infected with during storage or fabrication. So, a cleaning process was optimized to rid the sample of those surface impurities. This cleaning process will be done in 3 steps using RCA Procedure.

1. Removal of the organic contaminants (Organic Clean)
   1:1:5 solution of NH_4OH (ammonium hydroxide) + H_2O_2 (hydrogen peroxide)+H_2O (DI water) 10-15 min. at 80°C (created ~10Å silicon dioxide layer)
2. Removal of thin oxide layer (Oxide Strip)- We use 1:50 solution of HF (hydrofluoric acid) + H_2O (DI water) 1-2 min. at 25°C (created hydrophobic surface). Use a TEFLON BEAKER.
3. Removal of metallic contaminants (Ionic Clean)-
   We use 1:1:6 solution of HCl (hydrochloric acid)+H_2O_2+H_2O (DI water) 10-15 min. at 80°C

THERMAL OXIDATION:

Silicon dioxide may be grown on the substrates through either "Dry" or "Wet" thermal oxidation:

$$Si_{(solid)} + O_{2(gas)} \Rightarrow SiO_2 \quad \text{(DRY)}$$

Or

$$Si_{(solid)} + 2H_2O_{(vapor)} \Rightarrow SiO_{2(solid)} + 2H_{2(gas)} \quad \text{(WET)} \qquad (1)$$

The silicon is the sample itself in these reactions and therefore, some of it is used up in the growth of the oxide film. It can be shown from the densities and molecular weight of silicon and silicon dioxide that during the growth of an oxide layer with thickness x, a layer of silicon with thickness 0.45x is consumed. If we assume that a minimum oxide layer of 0.6 μm is required to prevent the formation of a junction in the silicon during diffusion, then the growth of such an oxide layer will consume 0.27 μm of silicon ... this can be neglected for our purposes. To determine the oxidation condition for the growth of this oxide layer with the "masking thickness" of x =0.6 μm, the following "parabolic relationship" can be used:

$$X_o^2 + A \cdot X_o = B \cdot t \qquad (2)$$

Where:

X_o = oxide layer thickness [μm].
t = oxidation time [hr].

B = parabolic rate constant [(μm)^2/hr].
= 0.4 (μm)^2/hr at T = 1000 °C for wet oxidation.
= 0.6 (μm)^2/hr at T = 1100 °C for wet oxidation.

B/A = linear rate constant [μm/hr].
= 0.647 μm/hr at T = 1000 °C for wet oxidation.
= 2.441 μm/hr at T = 1100 °C for wet oxidation.

Thus, if we want to grow 0.6 μm of oxide using wet oxidation with T = 1000 °C, we would require an oxidation time equal to:

$$t = \frac{(0.6\mu m)^2}{\left(0.4 \, (\mu m)^2 / hr\right)} + \frac{(0.6\mu m)}{\left(0.647 \, \mu m / hr\right)} = 1.827 hr = 109.64 \min = 1_{hr} : 50_{\min}$$

The oxidation is performed using the apparatus shown in figure 3. The samples are loaded on the quartz oxidation boat and placed in the center of the quartz oxidation reactor. The reactor temperature and gas flow should be adjusted before the loaded boat is positioned inside the chamber. For our initial oxidation, the temperature inside the reactor at its center is set to 1100 °C and the oxygen gas O_2 flow rate is set to approximately 4 CFH (1 CFH ~ 2 L/min). The O_2 is passed through a heated (96-100 °C) saturator filled with de-ionized (DI) water and is then piped through to the reactor input tube. Note that the "wrap-around" heater located at the reactor input serves to vaporize any liquid H_2O which is not caught by the condensation trap.

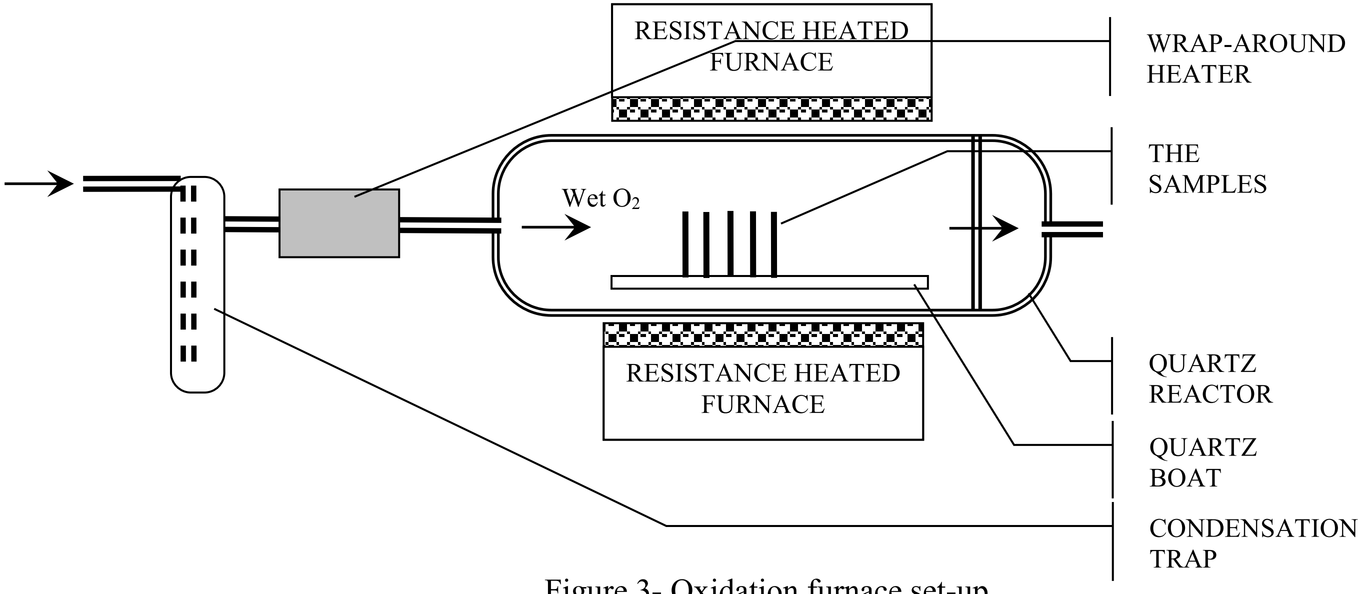


Figure 3- Oxidation furnace set-up

THE DIFFUSION PROCESS:

The diffusion process is a microelectronic fabrication process, through which we

can introduce a certain type of dopant impurities to the sample. The depth and concentration of the dopant can be controlled by the general diffusion equation:

$$D \cdot \left[\frac{\partial^2 N(x,t)}{\partial x^2} \right] = \frac{\partial N(x,t)}{\partial t} \quad (3)$$

Where:

N(x,t): ($1/cm^3$) is the impurity concentration at a certain depth (x) and diffusion time (t).

D: (cm^2/sec) diffusion coefficient of a given impurity at a given temperature.

The solution to this equation is highly dependable on the boundary condition process settings. Mainly, there are two kinds of boundary conditions process settings, the Predeposition diffusion process setting, and the Drive-In diffusion process setting. And since mostly every time the Predeposition process comes before the Drive-In diffusion process, we are going to start with it.

THE PREDEPOSITION DIFFUSION PROCESS:

Predeposition is a diffusion process by which a certain amount from the total dopant impurity atoms placed at desired region on the sample surface can be inserted into the sample bulk to a specific depth. Thus, by the end of this process we can measure the number of impurity atoms by their surface concentration ($1/cm^2$). The boundary condition for this type of diffusion is set as follows:

1- $N(x=0,t) = N_o$ = constant (usually the solid solubility or manufacturer specified)
2- $N(x=\infty,t) = 0$
3- $N(x,t=0) = 0$
4- D = constant

With respect to those conditions, the general diffusion equation will be solved using a numerical method to produce the following solution:

$$N(x,t) = N_o \cdot erfc\left[\frac{x}{2 \cdot \sqrt{(D \cdot t)_{\Pr edep}}} \right], (1/cm^3) \quad (4)$$

Where the Complementary Error Function (erfc[x]) is a well known numerical solution which have been rigorously tabulated.

Now for example, if we have an N-type sample and we want to dope it with Boron (p-type), the junction depth will be located at the point in the substrate where the impurity concentration, N(x,t), equals the background concentration, N_{BC}, of the sample. We therefore need the value of the background doping concentration of our samples before we can proceed with the calculation of our diffusion time.

N_{BC} can be calculated by using the value of average resistivity given by the supplier of the wafer. Notice that this equation can be used for a P-type substrate by

replacing the electron mobility by the hole-mobility in the denominator.

$$\bar{\rho} = \frac{1}{q \cdot \mu_n \cdot N_{BC}} \qquad (5)$$

Where:

q = electronic charge [$1.6x10^{-19}$ C]
μ_n = electron mobility [cm^2/V·sec]
N_{BC} = substrate background concentration [cm^{-3}]
$\bar{\rho}$ = Average resistivity [Ω·cm]

In order to solve for N_{BC}, the average value of the electron mobility should be used. For example if ρ = 1 Ω-cm, and μ_n=500 cm^2/Vs, we get N_{BC}=1.25 x 10^{16} cm^{-3}.

Before proceeding with the calculation of diffusion time, we must determine the diffusion coefficient of Boron at T = 1100 °C (i.e. our diffusion will be carried out at this temperature). From standard tables of diffusion coefficients we find that D = $2x10^{-13}$ cm^2/s (or 0.072 um^2/hr) at 1100 C.

Thus the following parameters may now be used to solve equation (4) for our diffusion time, t_{diff}:

X= Xj = 2.6 μm (this is our design value for the depth of the junction)
N_o(T=1100 C, Boron) = $3x10^{20}$ cm^{-3} (solid solubility of B in Si at T=1100 C)
D(T=1100 C, Boron) = 0.072 um^2/hr
N(xj,t) = N_{BC} = $1.25x10^{16}$ cm^{-3}

Replacing these values in equation (4) we get:

$$1.25 \times 10^{16} = 3 \times 10^{20} \cdot erfc\left[\frac{2.6}{2 \cdot \sqrt{(0.072) \cdot t}}\right]$$

$$4.266666667 \times 10^{-5} = erfc\left[\frac{4.844813951}{\sqrt{t}}\right]$$

$$4.266666667 \times 10^{-5} = 1 - erf\left[\frac{4.844813951}{\sqrt{t}}\right]$$

$$erf\left[\frac{4.844813951}{\sqrt{t}}\right] = 0.999957$$

Referring to an error function table, we get that for erf(z) = 0.999957, z ≅ 2.89.

$$\frac{4.844813951}{\sqrt{t}} = 2.89$$

$$t = t_{diff} = 2.81 hr \Leftrightarrow 2 hr \,\&\, 49 \min$$

Our PREDEPOSITION DIFFUSION conditions are therefore:

Xj = 2.6 um
T_{diff} = 1100 °C

t_{diff} = 2hr & 49min
Boron source: Borosilica gel
Atmosphere: 80% N_2, 20% O_2

The Borosilica gel is applied to the samples with a spinner @ 3000 rpm for 30 sec. The samples are then baked at 110 °C for 1 minute in air, after which they are ready for diffusion. The manufacturer of the gel claims that the thin coating applied to the surface of the sample will act as a constant source of boron for diffusion depths of up to 10 um. The manufacturer also advises the use of a ~20% O_2, ~80% N_2 atmosphere during the diffusion to prevent the formation of a so-called "brown stain" which has been proven to cause high contact resistance problems after metallization.

THE DRIVE-IN DIFFUSION PROCESS:

As the name suggests, in this process the impurity atoms that were placed at the surface in the Predeposition process will be diffused to desirable depth using the Drive-In process. Thus, with these two processes the amount of impurity atoms (concentration) and the depth of their penetration can be controlled. Also, with this process setting we can re-grow the previously etched oxide on the sample surface. The boundary conditions and the associated assumption of the Drive-In settings are listed as follows:

a- $\left.\frac{\partial N(x,t)}{\partial x}\right|_{x=\infty} = 0$, No loss of impurities to the growing oxide layer.

b- $N(x=\infty, t) = 0$, The sample is assumed to be very long (∞ crystal).

c- $N(x, t=0) = N_o \cdot erfc\left[\frac{x}{2\cdot\sqrt{(D\cdot t)_{predep}}}\right]$.

d- $(D\cdot t)_{Drive-In} >> (D\cdot t)_{Predep}$, The average depth of Predep is much less then Drive-In.

e- Total impurity atoms number is constant during the Drive-In.

f- D = constant.

With respect to those conditions, the diffusion equation will have the Gaussian profile as a solution. Thus, the form of the solution will be as follows:

$$N(x,t) = \left[\frac{Q}{\sqrt{\pi\cdot(D\cdot t)_{Drive-In}}}\right]\cdot e^{\left[\frac{-x^2}{4\cdot(D\cdot t)_{Drive-In}}\right]} \tag{6}$$

Where:

$\sqrt{(D\cdot t)_{Drive-In}}$: Is the average penetration depth of impurity atoms due to Drive-In (cm).

Q: is the number of impurity atoms inside the substrate per unit area at the end of the Predep process (atoms/cm^2).

$$Q = 2\cdot\left[\frac{\sqrt{(D\cdot t)_{Predep}}}{\pi}\right]\cdot N_o \tag{7}$$

As can be seen from step 8 in the process steps shown in figure 2, the samples must be re-oxidized after Base Predep diffusion in preparation for emitter diffusion. For our purposes, this will be done by changing the atmosphere in the reactor to wet O_2 at the end of the Predep diffusion time and performing a wet oxidation at 1100 °C for 1/2 hr. Therefore, the samples are kept in the furnace for a total time of $t_{Total\text{-}diff} = (t_{Predep\text{-}diff} = 2_{hr} : 49_{min}) + (t_{Driv\text{-}In\text{-}diff=oxid} = 30min) = 3_{hr} : 19_{min} = 3.32$ hr.

It can be shown that within 5 minutes after the change in ambient, a sufficiently large layer of SiO_2 is grown beneath the Borosilica layer that it can be assumed that N_o has been effectively "removed" from the sample's surface. Thus, during the last 30 minutes, the diffusion proceeds via a Gaussian distribution. The fact that the ambient is changed will not prevent the boron from diffusing any further in the substrate and therefore, our diffusion depth will be affected. Let us calculate how much farther xj will be located from our design value of 2.6 um.

As a first approximation, we will calculate this value by assuming an "erfc" distribution of the impurity during the oxidation; equation (4) can therefore be used:

$$1.25\times10^{16} = 3\times10^{20}\cdot erfc\left[\frac{X_j}{2\cdot\sqrt{(0.072)\cdot(3.32)}}\right]$$

$$\frac{X_j}{0.97783} = 2.89$$

$$X_j = 2.83\mu m$$

Hence, we can expect our diffusion depth to be about 0.23 μm deeper than expected. However, recall that during the growth of 1 um of SiO_2, 0.45 μm of Si is consumed. During the last half-hour at T = 1100 °C, about 0.5 μm of SiO_2 is grown and therefore, about 0.25 μm of Si is consumed. Subtracting this from xj = 2.83 μm, we find that our effective junction depth will still be located at roughly 2.6 μm even though the oxidation is performed after the diffusion time of $2_{hr} : 49_{min}$.

THE PHOTOLITHOGRAPHY PROCESS:

In microelectronic devices fabrication we some times need to selectively be able to subject a certain region of the sample to further fabrication processing but at the same time leaving the other regions virtually not affected. The photolithography process can enable us to do just that by modifying the sample surface using: a polymer substance called Photoresist (PR). The accessories are spinner, certain photo mask, mask aligner and exposure system, and PR developer solution. There are two type of PR, positive (PR^+) and negative (PR^-), we are going to use PR^+. The sample is spin-coated with PR^+ and then exposed to ultra-violet (UV) light. The photoresist from the area exposed to UV

light gets removed when kept in a developer solution.

Usually we need to etch a window in SiO_2 to deposit impurities or to make contact holes, and to do that we can use the following procedure:

Procedure:

1- Secure the sample on the spinner and turn the vacuum switch ON.
2- Blow the sample with N_2 gun, and then turn the spinner switch ON.
3- Using the dropper, deposit between 3-5 droops of PR^+ on the sample, then let it spin for 30 sec.
4- To make the PR^+ sets more firmly on the wafer surface, we "Soft Bake" it using the forced-air convection oven at 110 °C for up to 30 min.
5- Expose the wafer to UV light for 10 second under the desired photo mask. This is done with the mask-aligner/expose system located in the "yellow room". The mask usually contains some dark areas called "opaque", which will prevent the UV-light from hitting the wafer, and some transparent areas, which will let the UV light hit the sample causing the exposed PR^+ to become weaker.
6- The exposed PR^+ will be developed and removed by dipping the wafer in Microposit Developer for almost 1-3 min. Then we rinse the wafer in D.I. water for 15 sec and blow it dry with the N_2 gun.
7- Using the forced-air convection oven at 110 ^{0}C for 30 min we will "Hard Bake" the wafer in preparation for etching.
8- Repeat from step 1 to 7 for each sample.

SIO2 ETCHING:

Almost every time we do Photolithography, SiO_2 etching comes after it. The procedure that we are going to use this time is as follow:

Preparation:

a- Rinse clean two Teflon and two glass beakers.
b- Fill the glass beakers with DI water, and put a sample carrier in one of them, which we will use to store the samples after the end of this process.
c- Prepare a mix of 1:4 (25ml: 100ml) HF: NH_4F in one of the Teflon beakers.
d- Prepare a mix of 1:50 (3ml: 150ml) HF: H_2O in the second Teflon beaker.

Procedure:

1- Dip the sample in the HF: NH_4F Teflon beaker for 1-2 min.
2- Dip the sample in the HF: H_2O Teflon beaker and check for hydrophobic surface at the window opining on the sample, if sample still not hydrophobic then repeat from step 1.
3- Dip the etched sample in the glass beakers filled with DI water, then rinse it with DI water and store it in the second glass beakers.
4- Repeat from step 1 to 3 for each sample.
5- Remove the PR^+ from all the samples by dipping them in Acetone filled beaker (except when the next process is metallization of the sample, in this case we leave the PR^+ on the samples).

THE METALLIZATION PROCESS:

The Metallization is a microelectronic process, by which metal contact to the active parts of the wafer is established. The Metallization process can be carried on in the following manner:

1- Clean the samples by rinsing them thoroughly with DI water then dry them with N_2 gun.
2- Load the samples in the evaporation chamber as soon as possible. When the chamber has been properly evacuated (i.e. vacuum down to roughly 10^{-6} Torr), evaporate the aluminum onto the loaded samples. When the evaporation is completed, the samples may be kept in the vacuum chamber until further processing can be carried out.
3- Take out the samples from the evaporator, and prepare a beaker filled with Acetone.
4- Remove the excess aluminum (i.e., "Lift Off') by soaking the samples in the Acetone filled beaker and shaking it in a ultra-sonic vibrator. The acetone will cause the PR^+ to swell and thus dislodge or lift-off when placed in an ultrasonic cleaner.

To make an intimate contact between the metal contacts and the Si surface, we will use the Alloying furnace.

5- Dry the samples with the N_2 gun. Then load them into the alloying furnace.
6- Let N_2 gas flow through the sealed reactor tube for 2 min. While waiting, light the Bunsen burner at the reactor tube exhaust.
7- Turn ON the furnace (Variac set to 80) and begin monitoring reactor temperature. When temperature reaches 350 ^{0}C (about 20 min. after), change ambient to nitrogen/hydrogen ... ****make sure that the gas begins burning at the exhaust within 2 min. …if not, shut OFF H_2 and determine source of problem****
8- When a temperature of 450 ^{0}C is attained, begin alloy timing and reduce variac setting to ~69. Perform the alloying for a total of 30 minutes.
9- When the alloying is complete, shut OFF the furnace and allow the system to cool in an H_2 atmosphere until the temperature decreases to 350^{0}C. At that point, the ambient may be changed to N_2 and the Bunsen burner may be extinguished.
10- The samples may be removed from the reactor when the temperature decreases to below 80 ^{0}C. ****don't forget to shut OFF the N_2****

THE PROCEDURE:

SESSION #1:
1- Cut the pieces.
2- Clean the N-type samples using the RCA cleaning process.
3- Oxidize the N-type samples at T = 1100 °C for 1 hour using Wet O_2 oxidation process.

SESSION #2:

1- Perform the photolithography using mask #1 on the N-type samples. Mask #1 is shown in figure 4.
2- Open the base-diffusion window by etching away SiO_2.
3- Remove photoresist.
4- Deposit Borosilica gel and bake it at 110 ^{o}C for 1 minute.

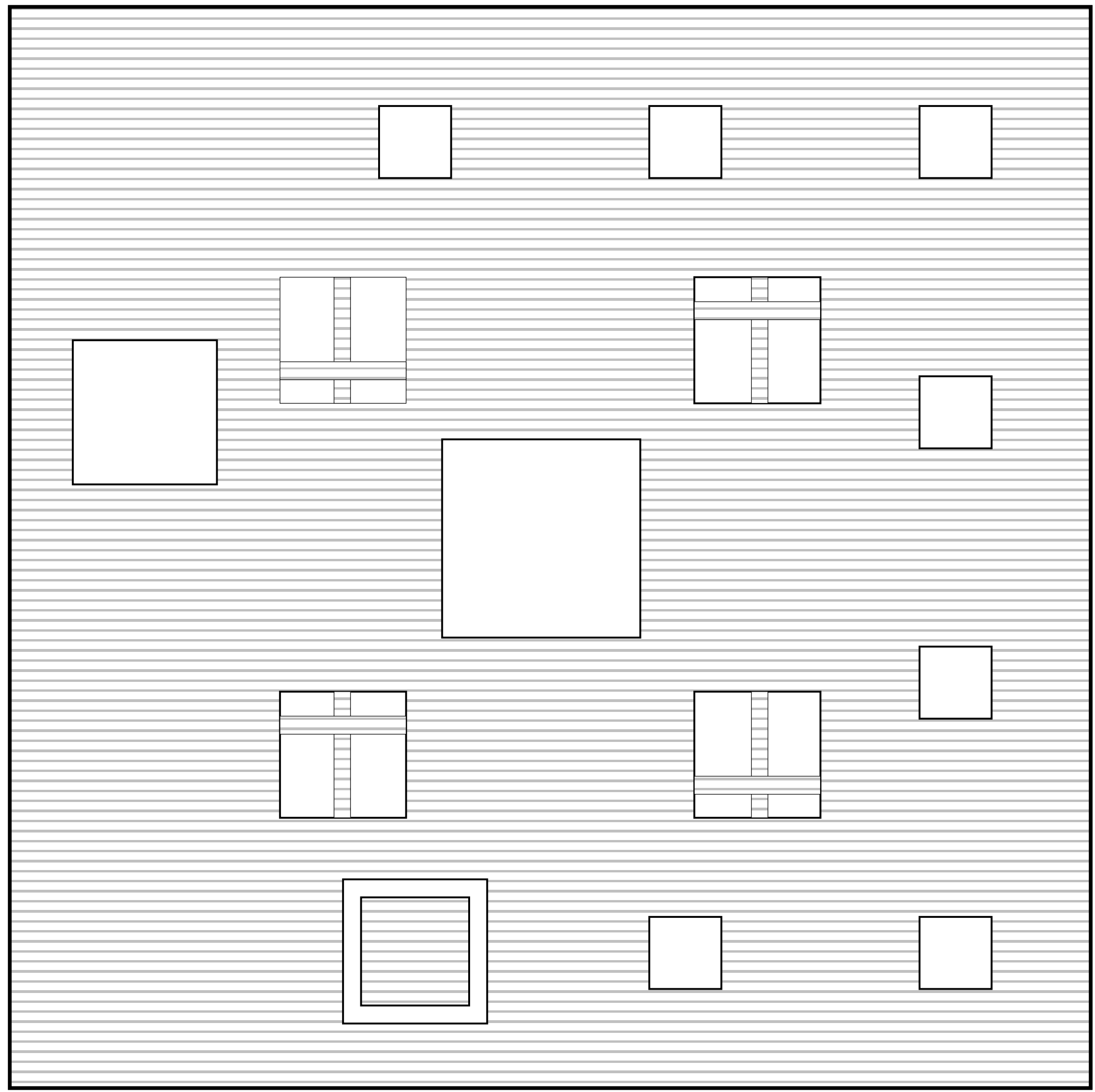
SESSION #3:
1- Diffuse the deposited Boron on the N-type samples at 1100 °C for 2 hour 49 min, using the Predeposition diffusion process settings.
2- Re-oxidize the samples at 1100 °C for 30 min.

SESSION #4:
1- Perform the photolithography of using mask #2 on the N-type samples. Mask #2 is shown in figure 5. This is for emitter and collector diffusion.
2- Open emitter and collector diffusion windows by etching away SiO_2.
3- Remove photoresist.
4- Deposit Phosphorosilica gel and bake it at 110 ^{o}C for 1 minute.

SESSION #5:
1- Diffuse the deposited Phosphorous at 1100 °C for 1 hour.
2- Re-oxidize at 1100 °C for 30_{min}, using the Drive-In diffusion process settings.
3- Perform the photolithography using mask #3. Mask #3 is shown in figure 6.
4- Remove oxide by etching.

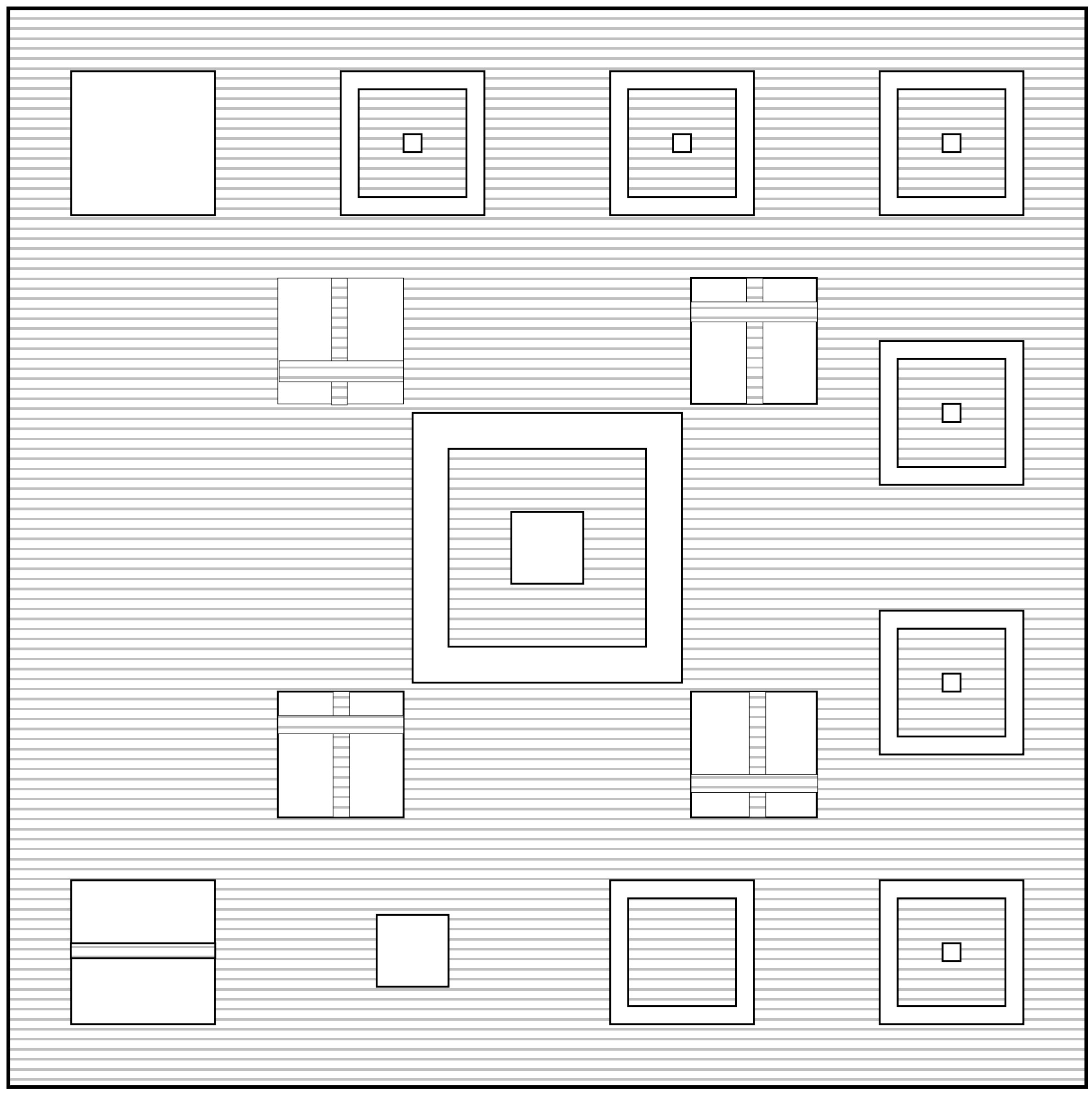
SESSION #6:
1- Deposit Al in the metal coater.
2- Do lift-off in acetone and then rinse in DI water.
3- Alloy the Al contact at 450°C for 30 minutes.

Note that figure 7 shows the complete layout of the sample when all the processes have been completed. The 3 masks used are shown in Figs. 4, 5, and 6.



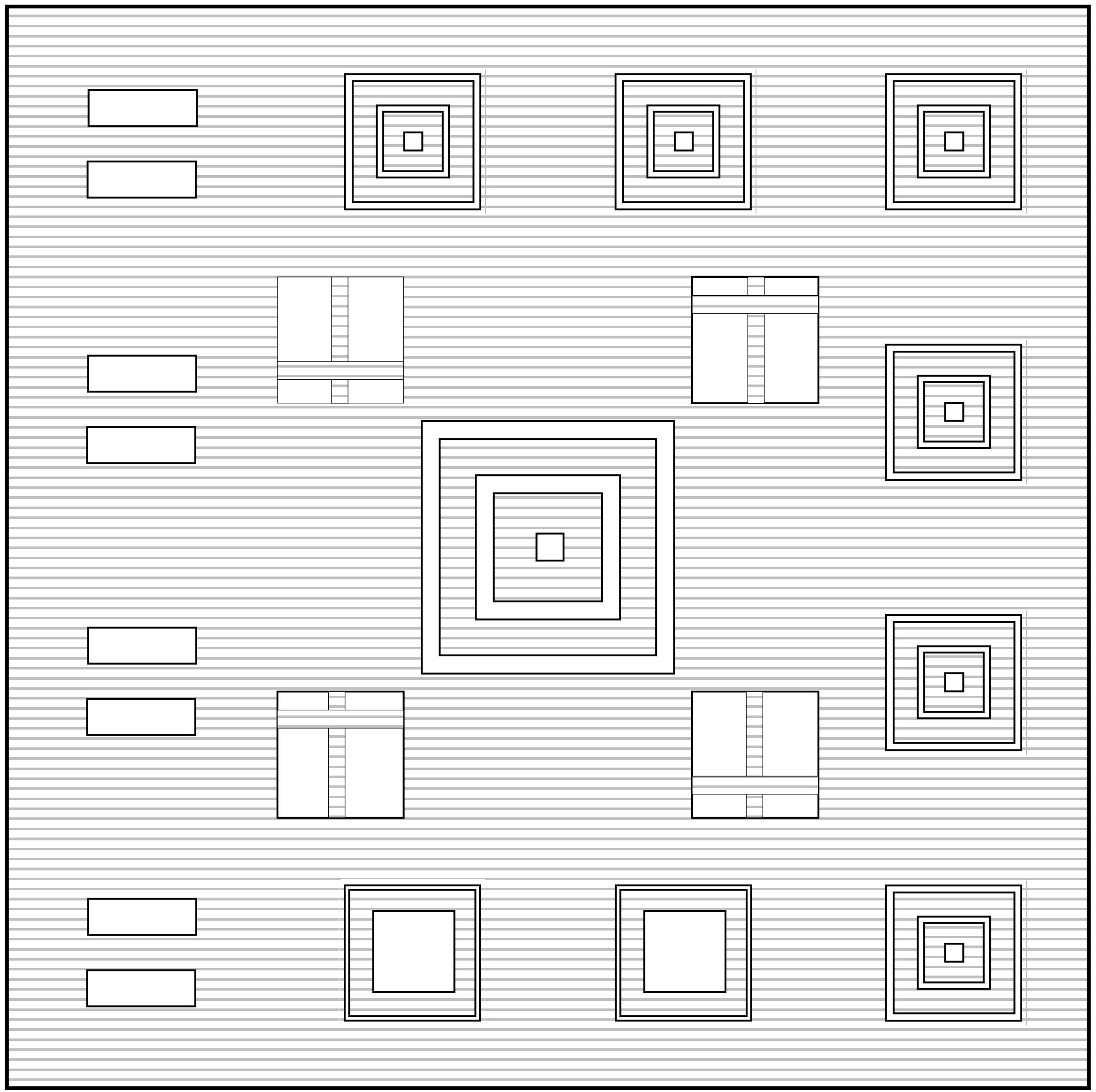
LEGEND:
1) GRID SPACING = 100 μm
2) GRIDDED AREA = OPAQUE
3) UNGRIDDED AREA = CLEAR

Figure 4; Mask # 1 (base diffusion)



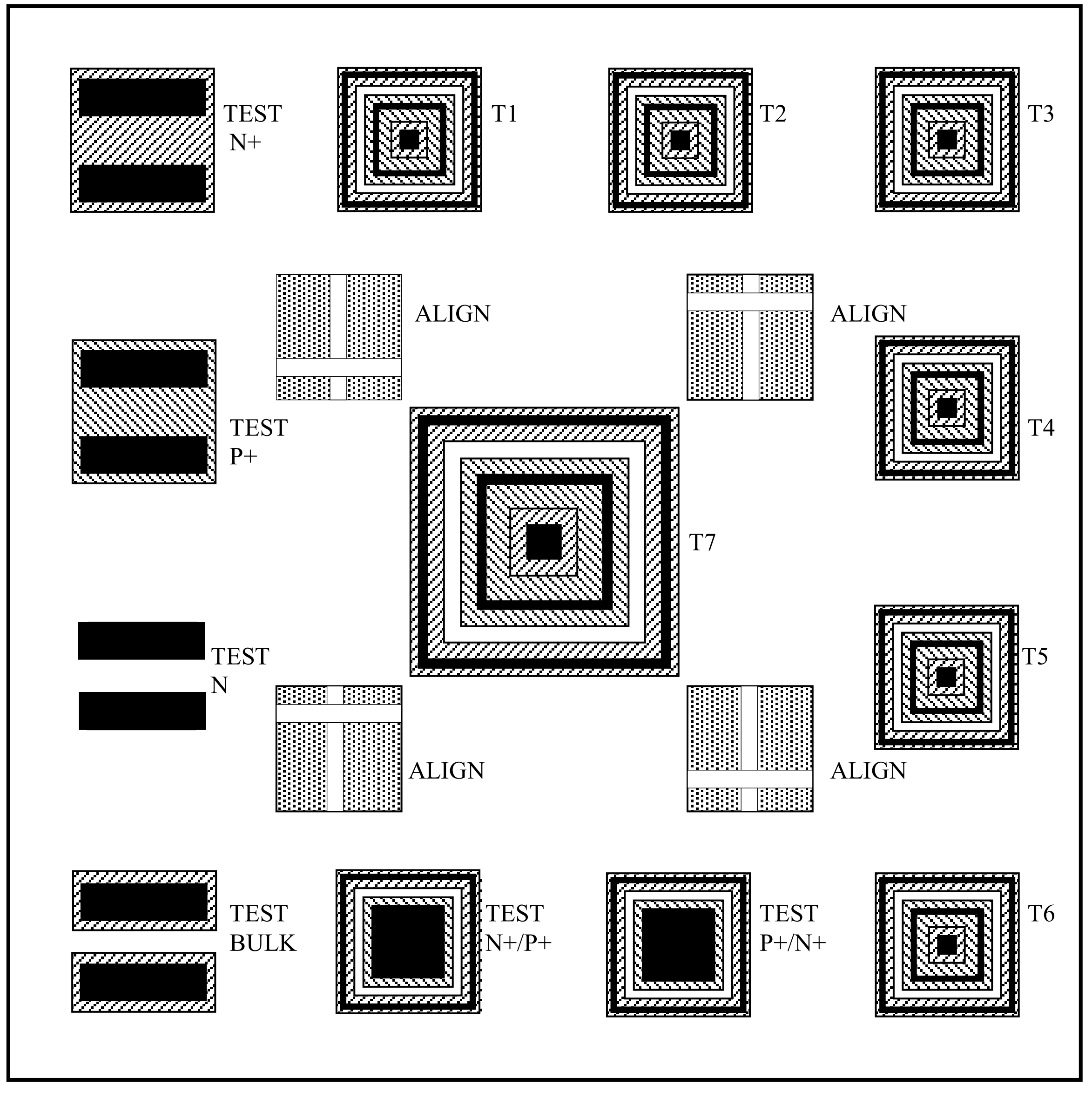
LEGEND:
4) GRID SPACING = 100 μm
5) GRIDDED AREA = OPAQUE
6) UNGRIDDED AREA = CLEAR

Figure 5; Mask # 2 (Emitter and Collector diffusion)



LEGEND:
7) GRID SPACING = 100 μm
8) GRIDDED AREA = OPAQUE
9) UNGRIDDED AREA = CLEAR

Figure 6; Mask # 3 (Metallization)



LEGEND:

- OXIDE
- ALL 3 LAYERS
- ALUMINUM
- N-TYPE DIFFUSION
- P-TYPE DIFFUSION

Figure 7; Device Layout